SPTS
A KLA Company

APPLICATION
BRIEF

Introduction to Si DRIE

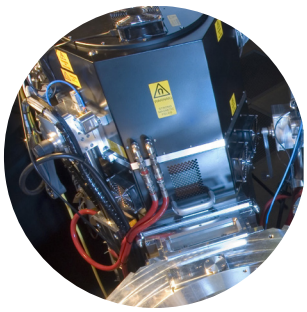
Introduction

SPTS Technologies has been at the forefront of deep silicon etch technology, since the invention of Deep Reactive Ion Etching (DRIE), also known as the "Bosch Process" in 1994. In conjunction with the inventors at Robert Bosch GmbH, SPTS developed the first commercial DRIE system for MEMS manufacturing, and have continued to innovate and improve the processing capabilities throughout the past 25 years. Prior to the invention of this technology the aspect ratio of a dry etched silicon feature was limited to ~10:1 using conventional non-switched techniques.

SPTS DRIE technology is used by the majority of leading MEMS manufacturers and foundries to etch deep vertical structures into silicon. In recent years, the applications for deep silicon etching have broadened to include through-silicon via (TSV) etching in advanced 3D packaging, trenches for silicon-based power devices and plasma dicing.

SPTS DRIE Process Modules

SPTS offers a choice of silicon DRIE modules. For most applications, our latest generation Rapier process module, with its "dual source" design, offers the best performance in terms of CD, profile and tilt control. Our DSi-*v* module offers higher etch rates and low non-uniformity for non-critical or high load cavity etching, and blanket silicon etching for via reveal or thinning.

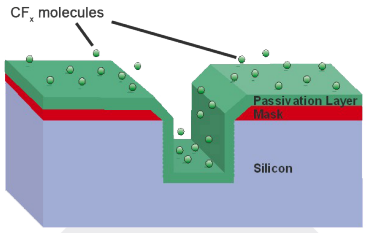


Omega® Rapier

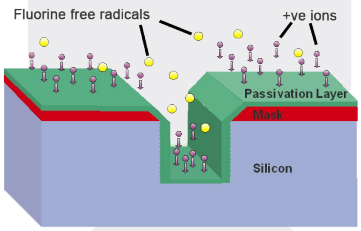
Omega® DSi-v

The Bosch Process

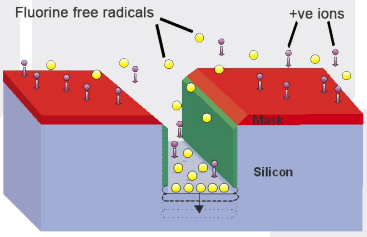
To create deep anisotropic etching of silicon, the Bosch Process switches between different plasma chemistries to provide fluorine based etching of the silicon while protecting the sidewall of the growing feature with a fluorocarbon layer. The schematic illustration below shows the 3 main steps of the process which are repeated multiple times to achieve a vertical etch profile. It is a complex but flexible plasma process with key process variables including gas flows, RF power, platen power, and switching times.



Step 1: A C_4F_8 plasma deposits a fluoropolymer passivation layer onto the mask and into the etched feature

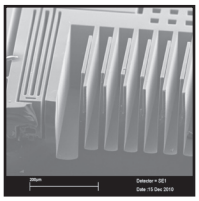
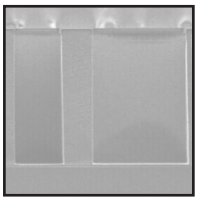
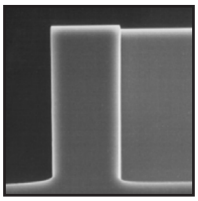
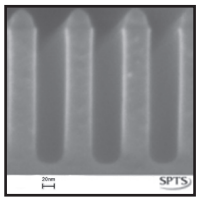
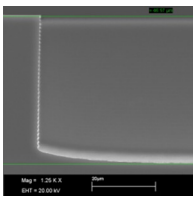
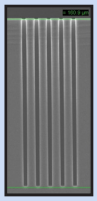
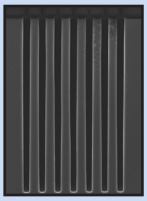
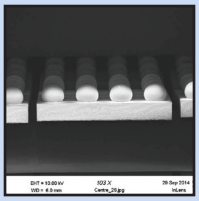
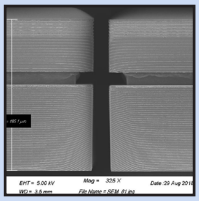
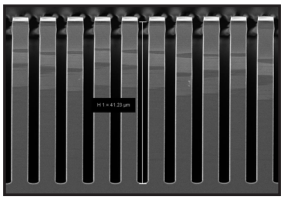


Step 2: A bias from the platen causes directional ion bombardment resulting in removal of the fluoropolymer from the base of the feature and the mask



Step 3: The fluorine free radicals, in the SF_6 plasma, etch the exposed silicon at the base of the etch feature isotropically, and so the process return to Step 1.

Applications for Si DRIE

Market	Applications	Typical requirements
MEMS	 *Low tilt*  *SOI etch*  *Smooth sidewalls*  *Nano features*  *Cavity etch*	
	High aspect ratio features	Vertical, smooth sidewalls No notching at SOI interface
	Microphone and other cavity etches	High etch rate (>30µm/min achievable) Sidewall usually less critical Low non uniformity
Advanced Packaging	 *0.4 x 36µm*  *4 x 160µm Sc <50nm*  *5 x 50µm Sc <70nm*  *8 x 180µm Sc <200nm*  *Plasma dicing bumped wafer*  *Plasma dicing bonded wafers*	
	Through-silicon via (TSV) etching	High etch rates with smooth sidewalls
	Plasma dicing	High etch rate Temperature management to prevent tape burn No notching at wafer-tape interface End-point detection
Power Devices	 *1.5 x 17µm Sc <22nm*  *3 x 40µm Sc <50nm*	
	Deep trench isolation	High aspect ratio, smooth sidewalls, Positive profile for dielectric deposition

End-point Options for Si DRIE

End-point control is important for optimizing silicon etch processes, but some features and pattern layouts can be challenging to monitor. SPTS offers a patented* end-point technology called Claritas™. Compared to standard on-chamber OES, Claritas™ provides process control of etches to a stop layer or buried cavities at low open areas (down to 0.05%) or high pressure processes that operate in the 100mT range.

*Patent US 9159599 B2

SPTS Technologies, A KLA company, designs, manufactures, sells, and supports etch, PVD, CVD and MVD® wafer processing solutions for the MEMS, advanced packaging, LED, high speed RF on GaAs, and power management device markets. For more information about SPTS Technologies, email enquiries@spts.com or visit www.spts.com